



Tech Notes

About Turbo Product Codes

Introduction:

The information here is compiled from different web sources, manufacturers and our own experience with the implementation of this relatively new FEC Technology. Turbo Product Codes has been in development for approximately 10 years with major work centered in France, Canada and the United States.

A primer on Turbo Product Codes is also available from Advanced Hardware Architecture in their Tech Note <http://www.chipcenter.com/networking/images/technote/technote008-appnote.pdf>.

Before Turbo Product Codes there were 3 major FEC techniques used in satellite communications, Sequential, Viterbi and concatenated Viterbi plus Reed-Solomon. Sequential is the oldest common technique and has given way to Viterbi FEC coding, perhaps mainly because several manufacturers make standard Viterbi chips, and the latency or bit delay through a Viterbi Codec is very low compared to Sequential. This can be very important when fast lock times are required at low data rates.

What TPC Promises, or What's all the Hoopla About:

Turbo Product Codes, or TPC, offers the best coding performance of any common FEC technology implemented to date. The performance is close to achieving the maximum possible coding performance as defined by the Shannon Limit.

A rate is a rate is a rate - The code rate for any FEC specifies the ratio of the number of data bits to the number of transmitted bits. This difference is the information added to the digital stream to allow error detection and correction. A rate 1/2 Viterbi convolutional FEC encoder transmits 2 bits for every bit of data. In other words only 50% of the transmitted bits are actually data. Every other bit is added information that allows the Viterbi decoder to determine if an error exists, and to correct the errored bit. A major point to consider here is that a rate 1/2 Viterbi FEC occupies the same bandwidth on the satellite as a rate 1/2 TPC FEC. What TPC does though is allow the same BER at a lower E_b/N_0 than Viterbi or Viterbi plus Reed-Solomon.

To achieve a lower bandwidth a lower code rate must be used. For instance a TPC rate 3/4 can be substituted for a Viterbi rate 1/2 and use approximately 40% less bandwidth with nearly the same BER vs. E_b/N_0 performance.

Different Implementations:

There are actually two different implementations of Turbo Codes. The first is called Turbo Convolutional Codes, or TCC, and the second is Turbo Product Codes or TPC. For FECs the label "convolutional" means that the redundant bits added into the data stream are "folded" into the stream. The classic Viterbi decoder operates on a convolutional data stream. In the case of Viterbi the data is never framed into blocks of data that are later processed. Convolutional Turbo Codes are

organized into blocks that are processed however the decoder process is different than that used in TPC. Some TCCs typically have a noise floor that limits the maximum BER achievable.

The most promising current implementation is Turbo Product Codes, or TPC. This methodology uses fixed blocks of data produced on the transmit side of the link and then decoded on the receive side to detect and correct errors.

Datum Systems uses the Turbo Product Codes implementation at rates 1/2, 3/4 and 7/8.

Pros and Cons:

In science, engineering and specifically communications you rarely get something for nothing. Most technology that improves information reliability is at the expense of either time or bandwidth. TPC is as close to something for nothing that we have seen. The tradeoff for superior performance is slightly longer latency involved in processing the blocks.

Compatibility - There is currently no hard standard for implementation of Turbo Product Codes, and the particular variables used by any company are likely to vary such that a TPC modem from one manufacturer is almost assured to not interface with any other brand. This may be resolved in the future by some manufacturer implementing compatible modes, or a governing body such as Intelsat releasing a standard implementation.

What We Offer:

Datum Systems' implementation of Turbo Product Codes offers the highest performance of any competing product we have seen. We use the latest available TPC processor by Advanced Hardware Architectures. The standard modes rates 1/2, 3/4 and 7/8 are optimized for BER vs. Eb/No performance. We also include rates 3/4 and 7/8 which use shorter block sizes and are optimized for lowest latency and demodulator lock times at a slight expense in performance.

To date we also believe that our prices are significantly less than any competitor's implementation of TPC.

Tech Note 6 in this section shows the classic BER vs. Eb/No "Waterfall" curves for all of our FEC technologies. These curves can be used to determine performance /comparison improvement for a link using any specific FEC.

MAB 11/11/01